REMARKS/ARGUMENTS

1. Rejection of claims 1-10 under 35 U.S.C. 102(b):

Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ota, US Patent Number 5,942,357.

This instant application claims are drawn to a reticle alignment procedure employed on a semiconductor wafer, a surface of the semiconductor wafer comprising a cell pattern area and a minor pattern area, the minor pattern area comprising at least one pre-layer wafer alignment mark (pre-layer wafer AM) transferred onto the semiconductor wafer from a pre-layer reticle-alignment mark (pre-layer reticle AM) on a pre-layer reticle, the reticle alignment procedure comprising: providing a current-layer reticle, the current-layer reticle comprising at least one current-layer reticle alignment mark (current-layer reticle AM) and a circuit pattern; performing a baseline check (BCHK) to align the current-layer reticle AM with the pre-layer wafer AM; capturing and comparing image signals of the current-layer reticle AM and the pre-layer wafer AM to calibrate a corresponding coordinate of the current-layer reticle to the semiconductor wafer; and performing a lithography process to simultaneously transfer layouts of the circuit pattern and the current-layer reticle AM onto the semiconductor wafer to form a current-layer wafer alignment mark (current-layer wafer AM) within the minor pattern area of the semiconductor wafer corresponding to the current-layer reticle alignment mark.

Ota describes, teaches and suggests all of the essential requirements of the claimed invention. Claim 12 is drawn to a method for determining an optimum baseline amount for an alignment sensor in an exposure apparatus for multiple-level exposure in which a photosensitive substrate is exposed at a plurality of positions disposed along an optical axis of the exposure apparatus adjacent to a best focused image, a baseline amount representing a positional relationship between a reference point with respect to which the alignment sensor detects a position of an alignment mark on the photosensitive substrate and a position of an image to be formed on the photosensitive substrate by the exposure apparatus, the method comprising the steps of: moving a fiducial mark relative to the best focused image in a direction substantially parallel to the optical axis of the projection optical system, the fiducial mark being moved to a plurality of vertical positions adjacent to the best focused image; at each of the plurality of vertical positions of the fiducial mark, detecting the fiducial mark through the alignment sensor to derive a baseline amount representing a position of the reference point of the alignment sensor relative to the position of the image which would be formed on the photosensitive if located at that vertical position; and processing data representing the baseline amounts detected at the plurality of vertical positions of the fiducial mark to derive the optimum baseline amount suitable for multiple-level exposure of the photosensitive substrate.

A more thorough description is given in the Specification at column 6, line 32, through column 7, line 44. Also at column 10, line 40, through column 11, line 5.

Based on this claim, and the teachings elaborated on in the

specification, claims 1-10 are anticipated by Ota.

Response:

Ota discloses a method for determining an optimum baseline amount by detecting a fiducial mark. A video reticle alignment (VRA) sensor is utilized to detect and compare a VRA mark formed on the fiducial mark with a VRA mark formed on a reticle R (Col. 7, lines 3-13). The present invention is characterized by using a VRA sensor to capture and compare image signals of a current-layer reticle alignment mark formed on the reticle with a pre-layer wafer alignment mark formed on the semiconductor wafer. Because Ota specifically teaches that the fiducial mark is installed on the wafer stage WS, instead of on the wafer W (Fig. 3, Col. 6, lines 58-59), the applicant believes that the fiducial mark taught by Ota cannot be read as the pre-layer wafer alignment mark formed on the semiconductor wafer as disclosed in claim 1 and claim 6 of the present application. Therefore, the method taught by Ota is believed different from the reticle alignment procedure of the present application.

From the aforementioned reasons, the applicant believes that claim 1 and claim 6 of the present application are absolutely different from Ota's disclosure. Reconsideration of the rejection over claim 1 and claim 6 is hereby requested.

As claims 2-5 and 7-10 are dependent upon claim 1 and claim 6, they should be allowed if claim 1 and claim 6 are allowed. Reconsideration of claims 2-5 and 7-10 is therefore requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: March 01, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan).